AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising an insulator layer having at least one of a via-hole for forming a via-stud and a trench for forming a wire ~~on a semiconductor substrate~~, wherein said one of the via-stud and the wire is formed ~~in said one of the via-hole and the trench through a barrier layer made of any one of an inorganic compound and a high melting point metal formed~~directly on inner surfaces of said one of the via-hole and the trench, through a barrier layer which is made of an inorganic compound or a high melting point metal, and wherein said one of the via-stud and the wire ~~being~~ is formed of said~~the same~~ metal ~~as a metal composing the barrier layer~~.

2. (Currently Amended) A semiconductor device comprising insulator layers having a via-stud and insulator layers having a wire ~~on a semiconductor substrate~~, said insulator layers having said via-stud and said insulator layers having said wire being alternately formed, wherein said via-stud and said wire are respectively formed in a via-hole and a trench ~~through barrier layers made of any one of an inorganic compound and a high melting point metal formed~~directly on inner surfaces of the via-hole and the trench, respectively, through a barrier layer which is made of an inorganic compound or a high melting point metal, and wherein

said via-stud and said wire ~~being~~ are formed of ~~the same~~ said metal ~~as a metal composing the barrier layer~~.

3. (Currently Amended) A semiconductor device comprising an insulator layer having at least one of a via-hole for forming a via-stud and a trench for forming a wire ~~on a semiconductor substrate~~, wherein said one of the via-stud and the wire is formed ~~in at least said one of the via-hole and the trench through barrier layers made of any one of an inorganic compound and a high melting point metal formed~~directly on inner surfaces of said one of the via-hole and the trench, through a barrier layer which is made of an inorganic compound or a high melting point metal, and wherein said one of the via-stud and the wire ~~being~~ is formed of ~~the same~~ said metal ~~as a metal composing the barrier layer~~ through electroplating after electroless plating of ~~the same~~ said metal.

4. (Currently Amended) A semiconductor device comprising an insulator layer having at least one of a via-hole for forming a via-stud and a trench for forming a wire ~~on a semiconductor substrate~~, wherein said one of the via-stud and the wire is formed ~~in said one of the via-hole and the trench through barrier layers made of any one of an inorganic compound and a high melting point metal formed~~ directly on inner surfaces of said one of the via-hole and the trench, through a barrier layer which is made of an inorganic compound or a high melting point metal, and wherein the whole of said one of the via-stud and the wire ~~being~~ is formed through electroless plating.

5. (Currently Amended) A semiconductor device comprising insulator layers having a via-stud and insulator layers having a wire ~~on a semiconductor substrate~~, said insulator layers having the via-stud and said insulator layers having the wire being alternately formed, wherein said via-stud and said wire are respectively formed in a via-hole and a trench ~~through barrier layers made of any one of an inorganic compound and a high melting point metal formed~~ directly on inner surfaces of the via-hole and the trench, respectively, through a barrier layer which is made of an inorganic compound or a high melting point metal, and wherein said via-stud and said wire ~~being~~ are formed of ~~the same~~ said metal ~~as a metal composing the barrier layer~~ through electroplating after electroless plating of ~~the same~~ said metal.

6. (Currently Amended) A semiconductor device comprising insulator layers having a via-stud and insulator layers having a wire ~~on a semiconductor substrate,~~ said insulator layers having said via-stud and said insulator layers having said wire being alternately formed, wherein said via-stud and said wire are respectively formed in a via-hole and a trench ~~through barrier layers made of any one of an inorganic compound and a high melting point metal formed~~directly on inner surfaces of the via-hole and the trench, respectively, through a barrier layer which is made of an inorganic compound or a high melting point metal, and wherein an entirety of said via-stud and an entirety said wire ~~being~~ are formed through electroless plating.

7. (Currently Amended) A semiconductor device according to claim 1, which includes said via-stud, ~~comprising an insulator layer having a via-stud on a semiconductor substrate, wherein said via-stud is formed in a via-hole through a barrier layer made of any one of an inorganic compound and a high melting point metal formed on an inner surface of the via-hole~~, and wherein a diameter of said via-stud ~~being~~ is smaller than 0.3 μm.

8. (Original) A resin sealed semiconductor device comprising a semiconductor device according to claim 7 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.

9. (Original) A resin sealed semiconductor device according to claim 8, wherein said spherical quartz particles are contained in the composition in an amount of more than 80 weight % of the total weight of said composition.

10. (Original) A module comprising a multilayer thin film wiring substrate composed of a plurality of laminated insulator layers, each of said insulator layers having a wiring layer on a surface; and a semiconductor device mounted on said wiring substrate, wherein said semiconductor device is the semiconductor device according to claim 9.

11. (Original) A large-scaled computer comprising a module substrate

mounted on a printed wiring board, said module substrate being connected to said printed wiring board through connecting pins; a multilayer thin film wiring substrate mounted on said module substrate, said multilayer thin film wiring substrate having a plurality of laminated insulator layers, each of the insulator layers having a wiring layer; and the semiconductor device according to claim 9 mounted on said wiring substrate.

12. (Original) A resin sealed semiconductor device comprising a semiconductor device according to claim 1 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.

13. (Original) A resin sealed semiconductor device according to claim 12, wherein said spherical quartz particles are contained in the composition in an amount of more than 80 weight % of the total weight of said composition.

14. (Original) A module comprising a multilayer thin film wiring substrate composed of a plurality of laminated insulator layers, each of said insulator layers having a wiring layer on a surface; and a semiconductor device mounted on said wiring substrate, wherein said semiconductor device is the semiconductor device according to claim 13.

15. (Original) A large-scaled computer comprising a module substrate mounted on a printed wiring board, said module substrate being connected to said

printed wiring board through connecting pins; a multilayer thin film wiring substrate mounted on said module substrate, said multilayer thin film wiring substrate having a plurality of laminated insulator layers, each of the insulator layers having a wiring layer; and the semiconductor device according to claim 13 mounted on said wiring substrate.

16. (Original) A resin sealed semiconductor device comprising a semiconductor device according to claim 2 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.

17. (Original) A resin sealed semiconductor device comprising a semiconductor device according to claim 3 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.

18. (Original) A resin sealed semiconductor device comprising a semiconductor device according to claim 4 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.

19. (Original) A resin sealed semiconductor device comprising a semiconductor device according to claim 5 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.

20. (Original) A resin sealed semiconductor device comprising a

semiconductor device according to claim 6 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.